Claims

1. A semiconductor package comprising:

a package substrate having a plurality of bond pads provided thereon;

a first semiconductor device mounted on the package substrate, the first semiconductor device having a plurality of bond pads provided thereon;

an interposer mounted on the first semiconductor device, the interposer having a first interposer bond pad and a second interposer bond pad, wherein the first and second interposer bond pads are electrically coupled;

a second semiconductor device mounted on the interposer, the second semiconductor device having a plurality of bond pads provided thereon;

a first bond wire connected to one of the plurality of bond pads on the first semiconductor device and to the first interposer bond pad; and

a second bond wire connected to the second interposer bond pad and to one of the plurality of bond pads on the second semiconductor device.

2. A semiconductor package in accordance with claim 1, further comprising a third bond wire connected to one of the plurality of bond pads on the package substrate and to one of the plurality of bond pads on the first semiconductor device.

3. The semiconductor package of claim 1, wherein the interposer comprises:

an interposer substrate;

a dielectric layer formed on the interposer substrate;

a conductive trace formed on the dielectric layer; and

a passivation layer formed on the conductive trace, said passivation layer having first and second windows formed therein to expose the conductive trace in areas defining the first and second bond pads.

4. The semiconductor package of claim 3, wherein the interposer substrate comprises silicon.

5. A stacked-die semiconductor package comprising:

a first semiconductor device having a top surface;

a second semiconductor device having a bottom surface and a top surface;

an interposer bonded between the top surface of the first semiconductor and the bottom surface of the second semiconductor, wherein the interposer includes a plurality of metal traces providing electrical connectivity between one or more interposer bond pads provided on the interposer;

a plurality of bond wires connecting one or more bond pads provided on the top surface of the first semiconductor device to one or more of the interposer bond pads; and

a plurality of bond wires connecting one or more interposer bond pads to one or more respective bond pads provided on the top surface of the second semiconductor device.

6. The stacked-die semiconductor package of claim 1, wherein the interposer comprises:

an interposer substrate;

a dielectric layer formed on the interposer substrate;

a conductive trace formed on the dielectric layer; and

a passivation layer formed on the conductive trace, said passivation layer having a plurality of windows formed therein to expose the conductive trace in areas defining the interposer bond pads.

7. The stacked-die semiconductor package of claim 6, wherein the interposer substrate comprises silicon.

8. A stacked die package comprising:

a package substrate having a top side and a bottom side, the top side having a plurality of bond pads provided thereon, and the bottom side having a ball-grid array pattern provided thereon;

a first semiconductor device mounted on the top side of the package substrate, the first semiconductor device having a plurality of bond pads provided thereon;

a silicon interposer mounted on the first semiconductor device, the interposer having a first interposer bond pad and a second interposer bond pad, wherein the first and second interposer bond pads are electrically coupled via a conductive trace, and wherein the interposer includes: an interposer substrate; a dielectric layer formed on the interposer substrate; a conductive trace formed on the dielectric layer; and a passivation layer formed on the conductive trace, said passivation layer having a plurality of windows formed therein to expose the conductive trace in areas defining the interposer bond pads; and

a second semiconductor device mounted on the interposer, the second semiconductor device having a plurality of bond pads provided thereon;

a first bond wire connected to one of the plurality of bond pads on said first semiconductor and to the first interposer bond pad;

a second bond wire connected to the second interposer bond pad and to one of the plurality of bond pads on the semiconductor device; and

a third bond wire connected to one of the plurality of bond pads on the top side of the package substrate and to a bond pad on the first semiconductor device.

9. A method for fabricating a semiconductor package comprising the steps of:

providing a package substrate having a plurality of bond pads provided thereon;

mounting a first semiconductor device on the package substrate, the first semiconductor device having a plurality of bond pads provided thereon;

mounting an interposer on the first semiconductor device, the interposer having a first interposer bond pad and a second interposer bond pad, wherein the first and second interposer bond pads are electrically coupled;

mounting a second semiconductor device on the interposer, the second semiconductor device having a plurality of bond pads provided thereon;

forming a first bond wire between one of the plurality of bond pads on the first semiconductor device and the first interposer bond pad; and

forming a second bond wire between the second interposer bond pad and one of the plurality of bond pads on the second semiconductor device.

10. The method of claim 9, further including the steps of forming a third bond wire between one of the plurality of bond pads on the package substrate and one of the plurality of bond pads on the first semiconductor device.

11. The method of claim 9, wherein the step of mounting an interposer includes the steps of: applying a layer of adhesive paste on the first semiconductor device;

placing the interposer on the layer of adhesive paste.

12. The method of claim 9, wherein the step of mounting an interposer includes the step of applying a portion of between the first semiconductor device and the interposer.

13. A method of fabricating a stacked-die package comprising the steps of:

providing a package substrate having a plurality of bond pads formed thereon;

providing a first semiconductor device and a second semiconductor device, each having a plurality of bond pads formed thereon;

providing an interposer, the interposer having a first interposer bond pad and a second interposer bond pad, wherein the first and second interposer bond pads are electrically coupled via a conductive trace, and wherein the positions of the first and second interposer bond pads and the conductive trace are selected to minimize the occurrence of crossing and interleaved bond-wires;

mounting the first semiconductor device on the package substrate;

mounting the interposer on the first semiconductor device;

mounting the second semiconductor device on the interposer;

forming a first bond wire between one of the plurality of bond pads on the first semiconductor device and the first interposer bond pad;

forming a second bond wire between the second interposer bond pad and one of the plurality of bond pads on the second semiconductor device; and

forming a third bond wire between one of the plurality of bond pads on the package substrate and one of the plurality of bond pads on the first semiconductor device.